A 0.8dB Insertion-Loss, 23dB Isolation, 17.4dBm Power-Handling, 5GHz Transmit/Receive CMOS Switch

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Abstract — **The highest performance to date of any switch using a CMOS process, of a 0.8dB insertion-loss, 23dB isolation and 17.4dBm power-handling capability at 5GHz, is accomplished with an optimized single-pole double-throw (SPDT) transmit/receive (T/R) switch using Depletion-layer-Extended Transistors (DETs) in a 0.18μm CMOS process. The effects of junction capacitance decrease and substrate resistance increase in the DET, the adoption of low-loss shielded-pads, and several layout optimizations, lead to the realization of this low insertion-loss. Moreover, the combined effect of the adoption of the source/drain DC biasing scheme and the high substrate resistance in the DET contributes to the high power-handling capability.**

I. Introduction

With recent significant improvement of RF performance of CMOS by rapid gate-length scaling, low-cost RF CMOS IC's are being studied and realized [1]. However, regarding an RF transmit/receive (T/R) switch, the existence of source/drain (S/D) junction capacitance (C_j) and conductive silicon-substrate results in severe RF-signal-loss, and therefore, realization of an adequate insertion-loss (I_L) switch, especially in a high-frequency range such as 5GHz, has been a big challenge [1]-[4]. Recently, we have proposed the Depletion-layer-Extended Transistor (DET) for the RF switch in a CMOS process and have realized a low I_L with significant C_j reduction and substrate resistance increase [5]. In this paper, we report the performance remarkably improved by applying several optimizations of the device parameters, the layout, and the circuit topology in the fabrication of the T/R switch utilizing the DETs in a 0.18μm CMOS process. Furthermore, through detailed investigation of inherent power-handling difficulties in a CMOS switch due to the existence of S/D junctions and the gate dielectric reliability issue, we were able to achieve high power-handling capability even with the utilization of high-performance 1.8V low-voltage operation transistors (Trs).

II. T/R CMOS Switch Utilizing DETs

The DET [5] possessing a new impurity profile has accomplished dramatic improvement of I_L in its RF switch operation, as shown in Fig. 1, and realized almost complete elimination of I_L degradation through the S/D C_j, which leaves I_L with the on-resistance of the Tr. In this work, an optimized single-pole double-throw (SPDT) T/R switch utilizing the DETs was fabricated in a 0.18μm CMOS process with four aluminum layers. A 10Ω·cm-resistivity silicon-substrate was used. The circuit diagram of this switch is shown in Fig. 2. A shunt/series type circuit was utilized to improve isolation characteristics at a high frequency of 5GHz. All four Trs were DETs, with a gate-length of 0.18μm and DC operation voltage of 1.8V. Gate-width (W) of each Tr was optimized using a circuit simulation analysis. That of the series Trs, T1 and T2, was 200μm and that of the shunt Trs, T3 and T4, was 100μm.

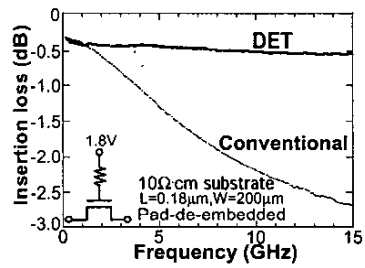

Fig. 1. Measured I_L of an individual DET as compared with that of the conventional N-channel MOS (NMOS) Tr. Both types of Trs were fabricated in a 0.18μm CMOS process. Pad effects were de-embedded.

As a circuit topology, the S/D DC biasing scheme [2,4] was utilized to improve power-handling capability. A DC bias was applied to the antenna port (ANT), the transmit

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port (TX), and the receive port (RX) with bias-Ts and to T3/T4 sources with the formation of capacitors C_{b1} and C_{b2} and resistors R_{b1} and R_{b2}. 1V was applied to S/Ds of all Trs ($V_{S/D}$=1V), and 2.8V and 0V were applied to V_{CTRL} and $V_{\overline{CTRL}}$. This voltage condition was determined with regard to power-handling capability enhancement and gate dielectric reliability limitation, as will be described later. Considering integration with a power amplifier operating in a power range of higher than 15dBm, 3.3V-operation Trs should be available as an optional process of the 0.18μm CMOS process. Therefore, the use of a DC voltage of less than 3.3V has been allowed in this design.

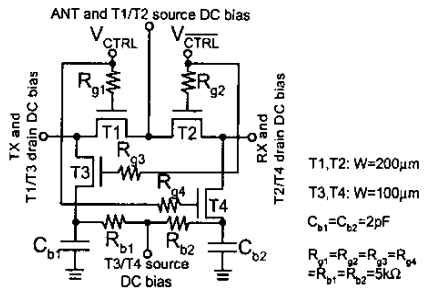

Fig. 2. Circuit diagram of fabricated shunt/series type T/R switch. 2pF capacitors, C_{b1} and C_{b2}, were formed with interdigitated capacitors [3], due to unavailability of metal-insulator-metal (MIM) capacitors in this fabrication. 5kΩ DC bias resistors, R_{g1}, R_{g2}, R_{g3}, R_{g4}, R_{b1} and R_{b2}, were formed with polysilicon resistors.

Moreover, optimizing pads and metal-interconnections is important to achieve a low I_L in the CMOS switch circuit. In this fabrication, ground-shielded pads whose ground-shield layers were formed using the silicided active areas [6] were adopted to improve I_L. Regarding metal-interconnections, low-loss 50Ω characteristic-impedance coplanar waveguide (CPW) transmission lines using only top metal layers were adopted. Since an RF power of more than 15dBm is inputted to the lines, their width was set to be as large as 14μm to satisfy the aluminum interconnection electro-migration reliability specification. Even with the use of these wide lines, the total loss from TX to ANT with the CPW lines in this fabrication was estimated by electromagnetic simulation and experimental confirmation to be as low as 0.1dB.

III. Experimental Results and Discussion

RF characteristics of the fabricated T/R switch were investigated. Figure 3 shows measured I_L and isolation characteristics of the switch between TX and ANT while terminating RX by 50Ω. This data contains the effects of pads and bonding-wires. A low I_L of 0.81dB was obtained at 5GHz in the on-mode of the switch. The I_L has been improved remarkably as compared with the first trial result [5] by loss reduction with adoption of the shielded pads, optimization of W of the Trs, and optimization of layout patterns, *e.g.*, metal-interconnection layout patterns and ground layout patterns. Figure 4 shows return-loss characteristics in the on-mode. The return-losses at TX and ANT at 5GHz were a high 23.8dB and 31.4dB, respectively, which are owing to the C_j reduction effect and substrate resistance increase effect in the DET. In the off-mode, the isolation was 23.4dB at 5GHz, which is high enough for the T/R switch because of the existence of the shunt Trs. Moreover, at a frequency of 2.4GHz, the I_L was 0.58dB and the isolation was 28.9dB.

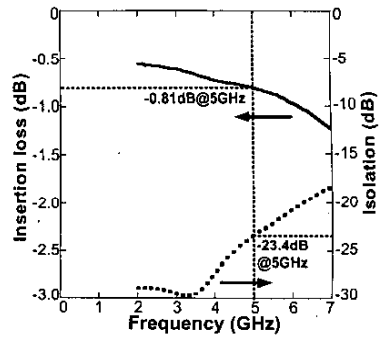

Fig. 3. Measured I_L and isolation characteristics of the T/R switch.

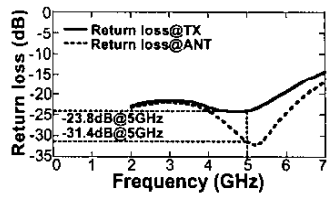

Fig. 4. Measured return-loss characteristics of the T/R switch.

Figure 5 shows measured power-handling capability characteristics at 5GHz in the on-mode of the switch. As mentioned before, the S/D DC biasing scheme [2] was adopted and the voltage condition of V_{CTRL}=2.8V, $V_{\overline{CTRL}}$=0V, $V_{S/D}$=1V was used. For reference, the data in the S/D zero-bias condition of V_{CTRL}=1.8V, $V_{\overline{CTRL}}$=0V, $V_{S/D}$=0V is shown in the same figure. Although the input power 1dB compression point (IP_{1dB}) was as low as 9.5dBm in the S/D zero-bias condition, the application of $V_{S/D}$=1V remarkably improved IP_{1dB} up to 18.6dBm. Considering the allowance of an I_L increase of 0.3dB in actual use and using a definition of input power 0.3dB compression point ($IP_{0.3dB}$), the $IP_{0.3dB}$ in the $V_{S/D}$=1V bias condition was 17.4dBm. It was also confirmed that no major degradation in the isolation characteristics occurs up to a power as high as 19dBm being inputted to the off-

mode switch. The results obtained in this work are summarized in Table I.

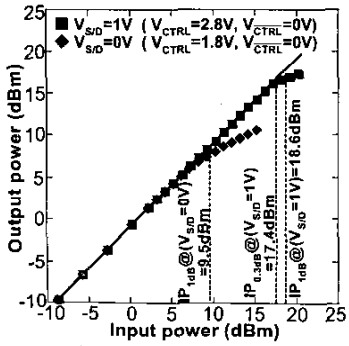

Fig. 5. Measured power-handling capability characteristics in $V_{S/D}$=1V case as compared with those in $V_{S/D}$=0V case.

TABLE I
PERFORMANCE SUMMARY OF T/R CMOS SWITCH

	Frequency	
Specification	2.4GHz	5GHz
Insertion loss	0.58dB	0.81dB
Isolation	28.9dB	23.4dB
Return loss	21.8dB	23.6dB
$IP_{0.3dB}$	—	17.4dBm
IP_{1dB}	—	18.6dBm

The following three issues limit the power-handling capability of a CMOS switch [2]. The first limitation is unintentional turning-on of the off-state Trs, where T3 is most severe. The second is unintentional turning-on of the S/D-to-body junction diodes in the off-state Trs by a forward biasing. The third is a gate dielectric reliability issue; that is, we have to suppress voltages across the gate dielectric of the Trs to guarantee their 10-year operation. The S/D DC biasing scheme improves the first two limitations. Here, Fig. 6 shows an equivalent circuit of the individual NMOS Tr with an external gate DC bias resistor in the off-state. In the DET, the ground-path substrate resistance, R_{si} is expected to be very high with the effect of the P-well removal [5]. Actually, from S-parameter characteristics fitting investigations, the R_{si} of the DET has been predicted to be higher than 1kΩ, which is far higher than the R_{si} of 20Ω in the literature [2,4]. The high R_{si} in the DET contributes to the IP_{1dB} improvement up to 18.6dBm in this work as compared with the reported results [2,4], in spite of the small S/D DC bias voltage of 1V. Namely, if the R_{si} is high enough, as in the DET case, the substrate side junction edge in Fig. 6 becomes a floating-node. At this time, the amplitude of the RF signal inputted to the drain is equally divided into V_{dj} and V_{sj} in the off-state Tr. On the other hand, in the case of a low R_{si}, the substrate side junction edge is weakly grounded and only the RF amplitude of V_{dj} becomes large, and therefore, this large RF amplitude of V_{dj} causes the above second limitation at the lower input power as compared with the DET case.

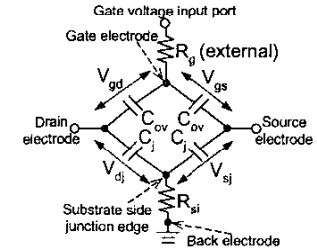

Fig. 6. Equivalent circuit of an NMOS Tr with an external gate DC bias resistor (R_g) in the off-state. C_{ov} is gate-to-S/D overlap capacitance. V_{dj} is voltage from substrate side junction edge to drain, V_{sj} is voltage from substrate side junction edge to source, V_{gd} is drain-to-gate voltage, and V_{gs} is source-to-gate voltage.

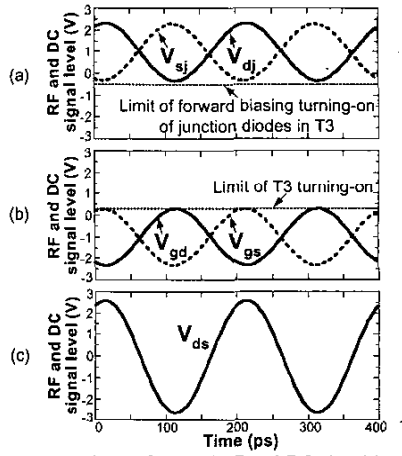

Fig. 7. Simulated waveforms of RF and DC signal levels in the off-state Tr of T3 at an input power of 17.4dBm, which is $IP_{0.3dB}$, in transmit-mode. (a) V_{dj} and V_{sj} in T3, (b) V_{gd} and V_{gs} in T3, and (c) source-to-drain voltage (V_{ds}) in T3. The Agilent Technologies Advanced Design System (ADS) microwave circuit simulator was used and a harmonic balance simulation was performed.

Figure 7 shows simulated waveforms of RF and DC signal levels in the off-state Tr of T3 at an input power of 17.4dBm in the transmit-mode. The following findings were obtained from this simulation result. First, as expected above with the high R_{si} effect in the DET, the simulated RF amplitude of V_{dj} is equal to that of V_{sj}. Second, the minimum voltages of V_{dj} and V_{sj} and the maximum voltages of V_{gd} and V_{gs} are -0.32V and 0.31V, respectively. Here, from other experimental results, it has been found that the junction diodes in the T3 begin to turn on at a V_{dj} or V_{sj} of around -0.5V and the T3 begins to turn

on at a V_{gd} or V_{gs} of around 0.3V. Therefore, it can be considered that at the input power of 17.4dBm, which is $IP_{0.3dB}$, the junction diodes do not begin to turn on, but the T3 does, and the simulated results are quite consistent with the experimental results. Third, the maximum voltages of V_{dj} and V_{sj} and the absolute values of the minimum and maximum voltages of V_{ds} are higher than 1.8V. However, this does not raise any reliability problem such as hot-carrier issues, since this T3 is in the off-state. Regarding the -2.3V of the minimum voltage of V_{gd} and V_{gs}, gate dielectric reliability has to be discussed. Namely, an RF signal stress whose DC offset is -1V and minimum voltage is -2.3V is applied to the thin film gate dielectric of the 1.8V-operation Tr. Here, its lifetime in this RF stress was estimated in the following way. Dividing an RF cycle into a large number of periods, the lifetime of each short period whose voltage is equal to the voltage amplitude of the original signal was estimated from time dependent dielectric breakdown (TDDB) characteristics of the gate dielectric. The estimated lifetime in the RF stress summing the lifetimes of all short periods was found to be sufficiently longer than 10 years.

Furthermore, voltage waveforms in the on-state Tr of T1, which are shown in Fig. 8, were also confirmed to be no problem in terms of reliability.

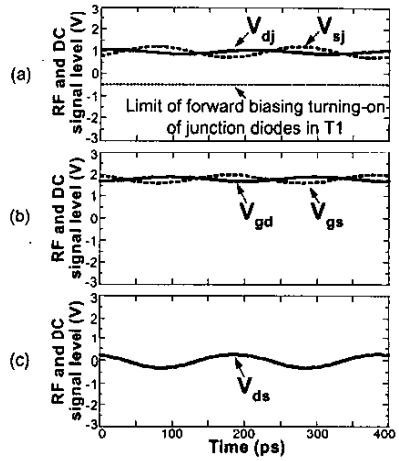

Fig. 8 Simulated waveforms of RF and DC signal levels in the on-state Tr of T1 at an input power of 17.4dBm in transmit-mode. (a) V_{dj} and V_{sj} in T1, (b) V_{gd} and V_{gs} in T1, and (c) V_{ds} in T1.

Finally, another reliability issue concerning an ANT load mismatch [2] has to be noticed. Considering the case in which the ANT load is open as the worst case, two times the RF voltage amplitude of that with a 50Ω load has to be endured. However, as understood from Fig. 7, a self-protecting effect, in that turning-on of both Trs and forward-biased junction diodes clips the signal while inputting an extremely high power signal, is expected. In fact, the following reliability test was performed. An input power stress of 23.4dBm with a 50Ω load, corresponding to two times the voltage amplitude of that at a power of 17.4dBm with a 50Ω load, was applied to ANT for one hour, after which no major change in the S-parameter characteristics between before and after the stress was observed. It is concluded from all the above reliability examinations that this switch will be able to handle a 17.4dBm input power without any reliability concern.

IV. Conclusion

A very low insertion-loss of 0.8dB has been achieved at 5GHz with the optimized SPDT T/R switch utilizing the DETs in a 0.18μm CMOS process. With the adoption of low-loss shielded-pads and CPW transmission lines, and several layout optimizations, this low I_L has been achieved by exploiting the effects of the DET. As for power-handling capability, a high IP_{1dB} of 18.6dBm and $IP_{0.3dB}$ of 17.4dBm have been achieved with the combined effect of the S/D DC biasing and the high R_{si} in the DET. With detailed investigations of the reliability issues, it has been found that this switch will be able to handle a 17.4dBm input power without any reliability concern.

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